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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,905	12/12/2003	Yean-Yow Hwang	15114-067400US	2440

26059 7590 12/02/2005

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,905	HWANG ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2005 and 14 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to Amendments & Remarks filed on 09/30/2005 regarding to application 10/734,905 filed on 12/12/2003. Claim 5 has been cancelled without prejudice. Claims 1 – 4 and 6 – 15 remain pending in the application.

Claim Objections

2. Claim listed below is objected to because of the following informalities:

Claim 13, line 7, after "wherein" insert **—the netlist performed by—**.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 4, 6, 7 and 13 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,594,657 to *Cantone et al.* over IEEE Paper entitled "*On Area/Depth" Trade-Off in LUT-Based FPGA Technology Mapping*" authored by *Cong & Ding* in view of U.S. Patent No. 6,088,262 to *Nasu*.

5. As to Claim 1, *Cantone et al.* show and teach the following subject matter:

- *Computer aided design* (CAD) system for implementation of FPGA – [col. 1, line 11 – 18; Fig. 1];
- User *entering* (i.e., *providing*) CAD system a *High-level application netlist language* (i.e., *high-level design language*) *description of a (logic) circuit* – [col. 3, line 15 – 25]; High level circuit description – [abstract]; specifying a *Boolean function* (i.e., *logic function*) using *Boolean equation* (i.e., *high-level design language*) – [col. 14, line 20 – 25]; logical gate – [col. 14, line 38]; Notice that (1) a *logic circuit* can be described by a *logic function* (*Boolean function*) using a *Boolean equation* (*high-level design language*) (2) the *logic function* can be synthesized using *logic gates* including AND, OR, INV, NAND, NOR etc.

Cantone et al. do not teach (1) synthesizing logic gates to respectively obtain a *first alternative netlist* and a *second alternative netlist* for the *logic function*, (2) performing a *technology mapping* of the *first alternative netlist* to obtain a *first mapping netlist* and performing a *technology mapping* of the *second alternative netlist* to obtain a *second mapping netlist* (3) selecting one of the corresponding *first mapping netlist* or *second mapping netlist* based on *design criteria*. But *Cong & Ding* teach *depth-optimal mapping* and *area-minimizing mapping* of a Boolean circuit using *lookup-table (LUT) based FPGA technology mapping* – [title; abstract].

Cong & Ding show and teach the following subject matter:

- Synthesizing *logic gates* (i.e., NAND and NOR) to obtain a *first alternative netlist* for a *logic circuit*, which can be expressed by a *logic function* – [Fig. 2(a)]; Notice that the *depth* of the *first alternative netlist* is 7;
- Performing *depth-optimal technology mapping* of the *first alternative netlist* to obtain a *depth-optimal mapping solution* (i.e., *first mapping netlist*) of depth 2, using 6 LUT's – [Fig. 2(b)];
- Synthesizing *logic gates* (i.e., NAND and NOR) to obtain a *second alternative netlist* for the same logic circuit; Notice that (1) for current study, the gate configuration of the *second alternative netlist* is the same as that of the *first alternative netlist* (2) the gate configurations of the *first alternative netlist* and

the *second alternative netlist* can be different if structural gate decomposition is applied;

- Performing *area-optimal technology mapping* of the *second alternative netlist* to obtain an *area-optimal mapping solution* (i.e., *second mapping netlist*) of depth 5, using 6 LUT's – [Fig. 2(b)];
- Good/optimal mapping solutions under different *optimization objectives* (i.e., *design criteria*) – [page 137, right column].

Notice that selection of the *first mapping netlist* (*depth-optimal mapping solution*) or *area-optimal mapping solution* is based on *design criteria* (i.e., *depth-optimal objective* or *area-optimal objective*) of the logic circuit. *Cong &Ding* also teach that, using graphical representations, a set of visible mapping solutions for a given (logic) design can be obtained in order to select a mapping option to meet various area and depth requirements – [page 138, first paragraph on left column].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Cong & Ding* in utilizing graphical representations to generate a set of visible mapping solutions for a given (logic) design in order to *select a mapping option* to meet various area and depth requirements thereby achieving a *selected mapping netlist*.

In addition, *Cong & Ding* also teach the following subject matter:

- First mapping netlist comprises a plurality of logic gate array block – [Fig. 2(b)];
- *Re-mapping* for area minimization – [page 138, left col., second paragraph]; *area/depth trade off* in LUT-based FPGA technology mapping – [title]; Notice that the (1) Re-mapping can also be applied for depth minimization (2) *re-mapping*, *area/depth trade off* is applied for *optimizing* the *selected mapping netlist*;
- After optimizing, performing a *technology mapping*, *using RAM memory to realize each LUT*, on the *selected mapping netlist* – [col. 18, line 59 – 67].

The *first alternative netlist* shown in Fig. 2(b) of *Cong et al.* comprises logic gates.

Cong & Ding shows in Fig. 2(b) that the *first mapping netlist* comprises logic *gate array blocks.* Although *Cong & Ding* and *Cantone et al.* do not teach that the logic gate array blocks are *digital signal processing blocks*, it is well known in the art that a logic *gate array block* can be designed to perform a digital signal processing function – [See teachings disclosed by *Nasu*: col. 12, line 46 – 51]. Notice that a *logic gate array block* having digital signal processing function is a *digital signal processing block*. Therefore, a technology mapping can be applied on a plurality of *digital signal processing blocks* to obtain a first mapping netlist in processes of optimization in order to meet various area and depth requirements in design of desired *digital signal processing blocks*.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claims 2 and 3, reasons are included in **[Response A]** given above. Notice that *depth-optimal mapping* is equivalent to *delay-optimal mapping*; optimizing delay is achieved by optimizing depth.

7. As to Claim 4, reasons are included in **[Response A]** given above. The *first mapping netlist* shown in Fig. 2(b) comprises LUT structures, whose logic functions are represented by a set of logic blocks made of logic gates.

8. As to Claim 6, reasons are included in **[Response A]** given above.

9. As to Claim 7, reasons are included in **[Response A]** given above.

10. As to Claim 13, reasons are included in **[Response A]** given above. Notice the following:

- a *netlist* ⇔ a *first alternative netlist* or a *second alternative netlist*;
- a *first technology mapping* ⇔ a *depth-optimal technology mapping* or a *area-optimal technology mapping* of netlist into gate array blocks, which are to be implemented using LUT's;
- a *synthesis optimization* ⇔ *area/depth trade-off* on the netlist;

- a *second technology mapping* ⇔ LUT realization of gate array blocks using RAM memory.

11. As to Claim 14, the *first technology mapping* maps the netlist to a *LUT-based FPFA*, which is the same target technology (LUT-based FPGA) as the *second technology mapping*.

12. As to Claim 15, reasons are included in **[Response A]** given above.

13. Claims 8 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,594,657 to *Cantone et al.* and of IEEE Paper entitled "*On Area/Depth" Trade-Off in LUT-Based FPGA Technology Mapping*" authored by *Cong & Ding* and U.S. Patent No. 6,088,262 to *Nasu* in view of IEEE Paper entitled "*Structural Gate Decomposition for Depth-Optimal Technology Mapping in LUT-Based FPGA Designs*" authored by *Cong & Hwang*.

14. As to Claim 8, in addition to reasons included in **[Response A]** given above, *Cantone et al.* and *Cong & Ding* show and teach the subject matter with the following equivalences:

- *generating* a *first alternative netlist* for a *logic function* ⇔ *synthesizing* a *first alternative netlist* (e.g., depth-optimal LUT-based netlist) for a *logic function*;
- *generating* a *second alternative netlist* for the *logic function* ⇔ *synthesizing* a *second alternative netlist* (e.g., area-optimal LUT-based netlist) for the *logic function*;
- Selecting one of the *first alternative netlist* or the *second alternative netlist* as a *selective alternative netlist* based on results of a *technology mapping* (i.e., LUT-based technology mapping) of the *first alternative netlist* and the *second alternative netlist* – [**Response A**; Cong & Ding: Fig. 2].

Cantone et al., *Cong & Ding* and *Nasu* do not teach that *gate configuration* of the *second alternative netlist* is different from that of the *first alternative netlist*. But *Cong & Hwang* teach structural gate decomposition for depth-optimal technology mapping in LUT-based FPGA designs – [title; abstract]. Notice that the structural gate

decomposition is applied to change the *gate structure* of a given logic circuit. *Cong & Hwang* also teach that *structural gate decomposition* is performed on netlist of a logic circuit in order to allow mapping algorithms to obtain the *smallest mapping depth* – [page 196, second paragraph].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Cong & Hwang* in performing *structural gate decomposition* on the *first alternative netlist* of the logic circuit under study in order to allow mapping algorithms being utilized thereby achieving the *smallest mapping depth*.

Notice that, when the *structural gate decomposition* is performed on the *first alternative netlist*, the gate configuration of the *first alternative netlist* is different from that of the *second alternative netlist*.

For reference purposes, the explanations given above in response to Claim 8 are called **[Response B]** hereinafter.

15. As to Claim 9, reasons are included in **[Response A]** given above. As explained in **[Response A]**, *depth-area trade-off* is performed by *re-mapping* a netlist for optimization; it is applied to perform a *synthesis optimization* on the selected alternative netlist to obtain an optimized selected alternative netlist.

For reference purposes, the explanations given above in response to Claim 9 are called **[Response C]** hereinafter.

16. As to Claim 10, reasons are included in **[Response A]**, **[Response B]** and **[Response C]** given above. Notice that a technology mapping

17. As to Claims 11 and 12, reasons are included in **[Response A]** and **[Response B]** given above.

Response to Amendment and Remarks

18. Applicants' amendment and remarks filed on 09/30/2005 have been reviewed. Due to newly found prior art, responses cited in the Office Action mailed to the applicants on 03/11/2005 are reversed. Detailed responses are given above.

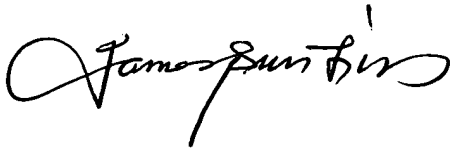
Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
November 29, 2005



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OK
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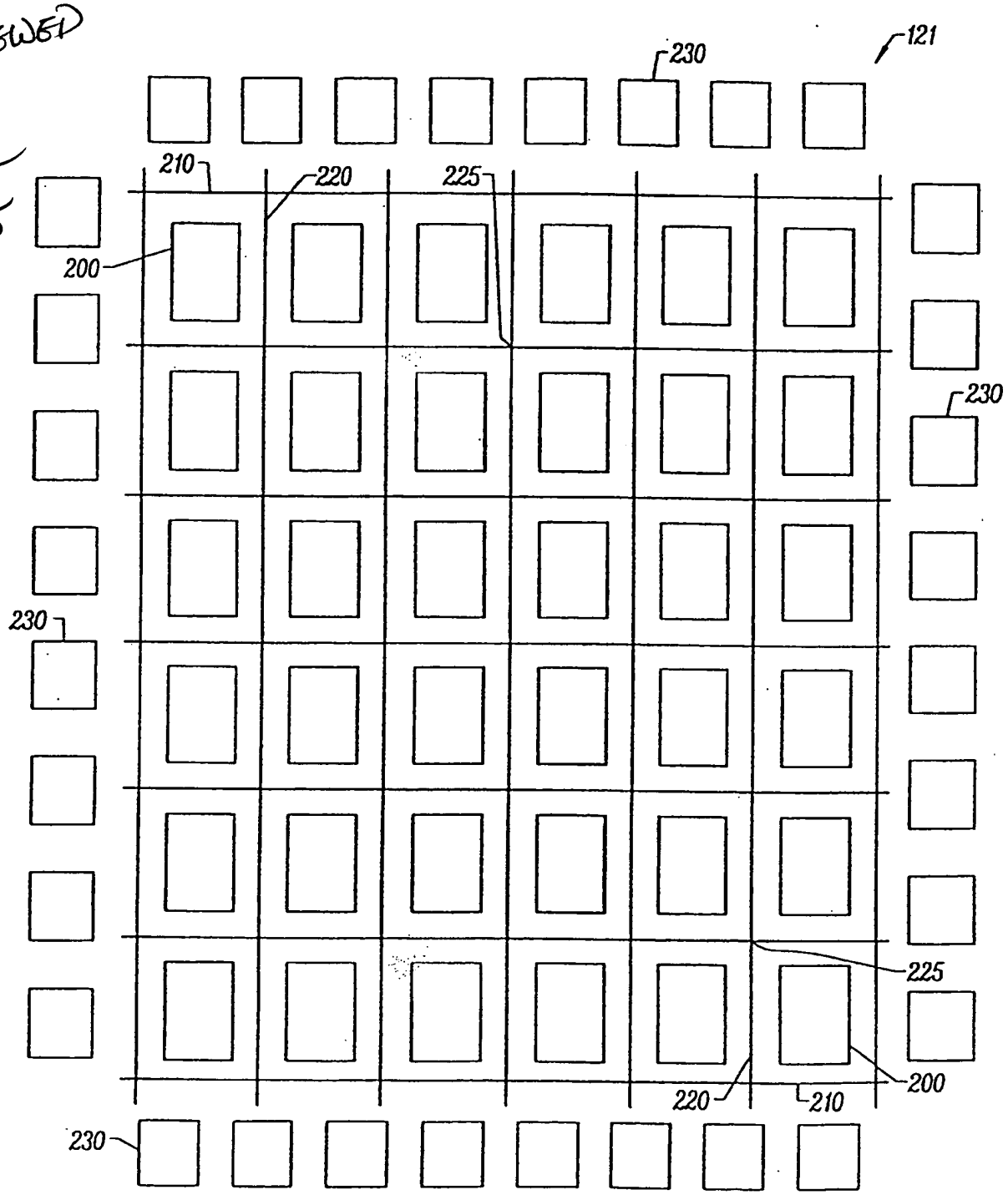

FIG. 2 (PRIOR ART)

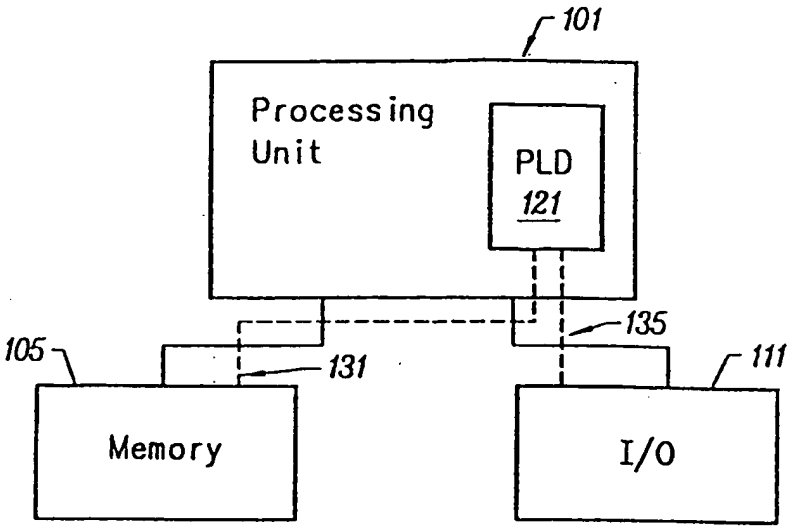

FIG. 1C

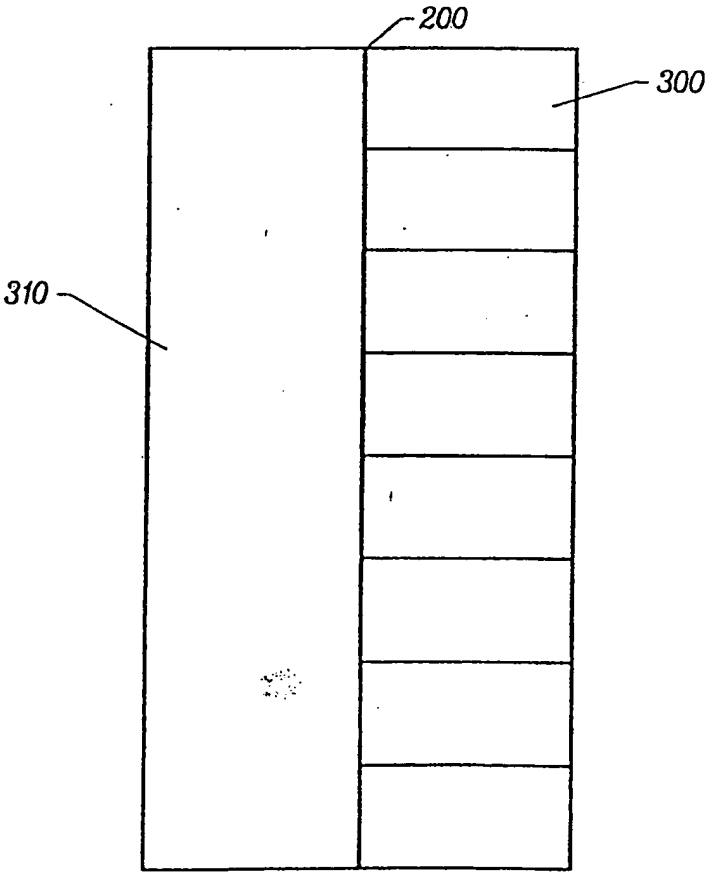

FIG. 3 (PRIOR ART)

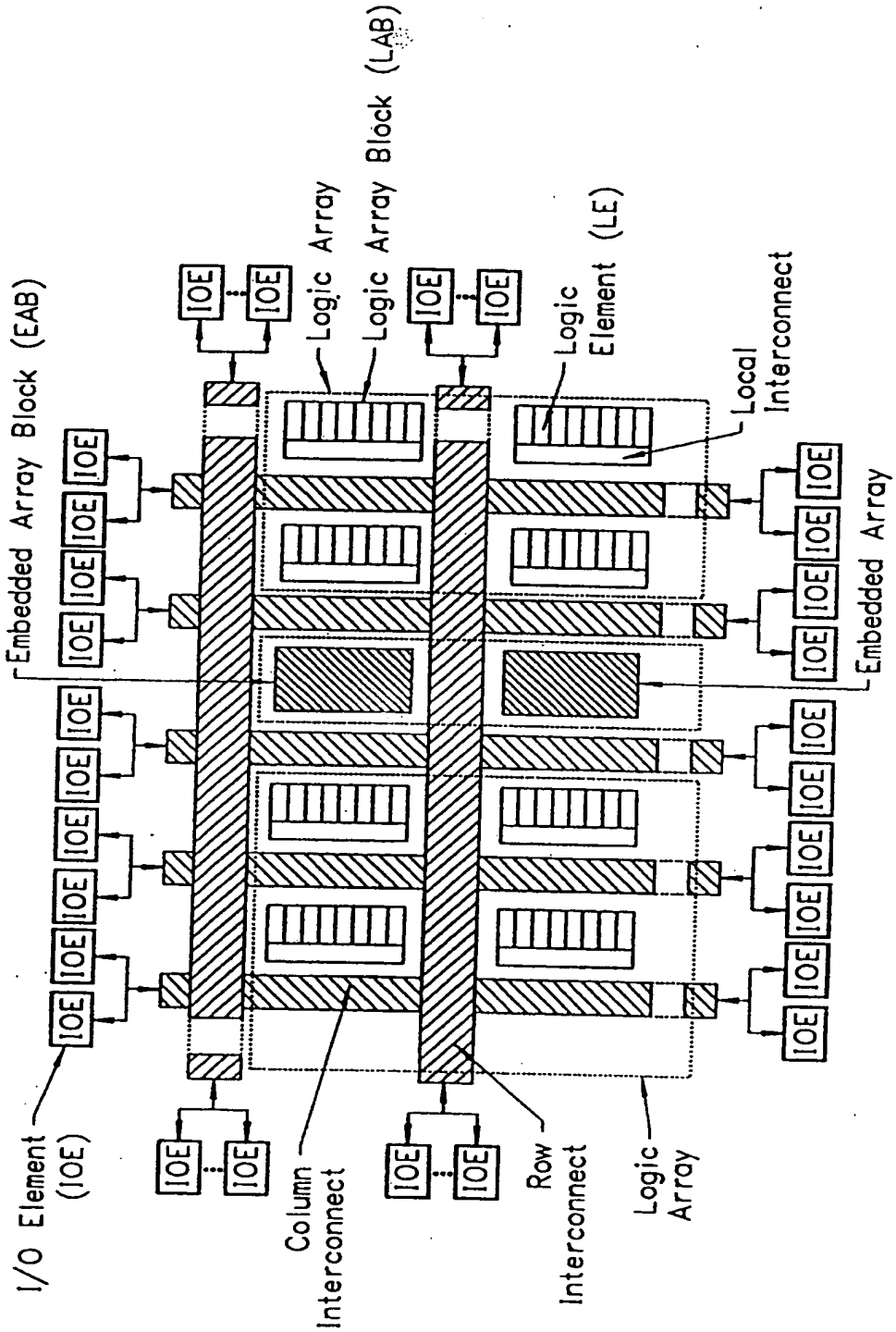

FIG. 4 (PRIOR ART)

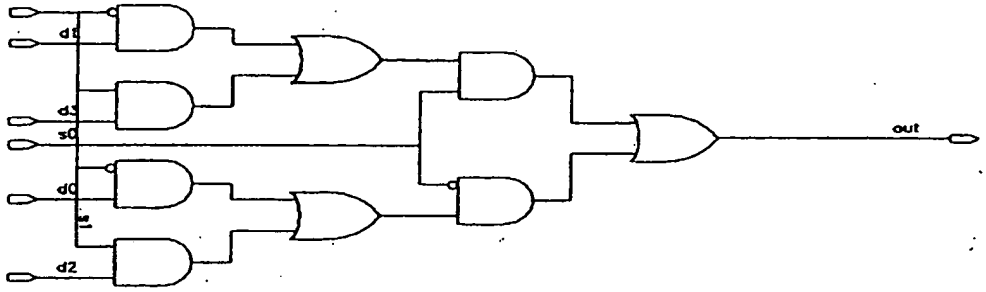

FIGURE 7 (PRIOR ART)

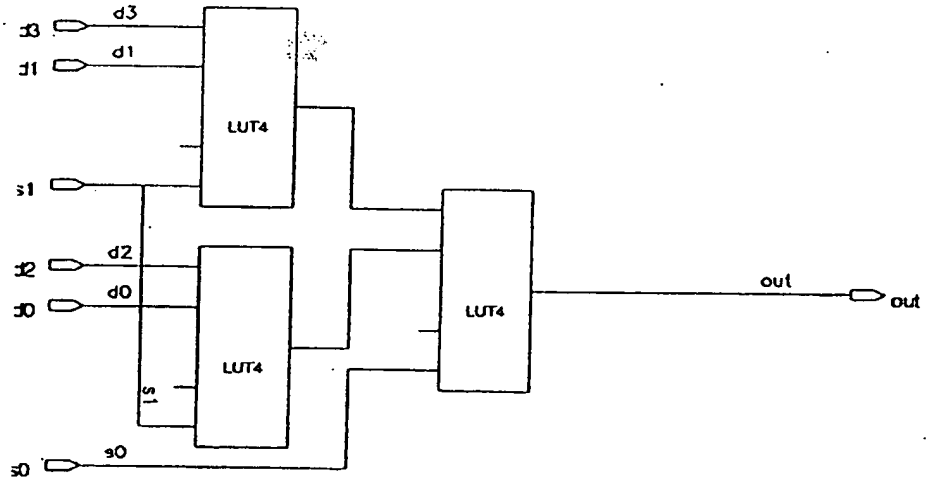

FIGURE 8

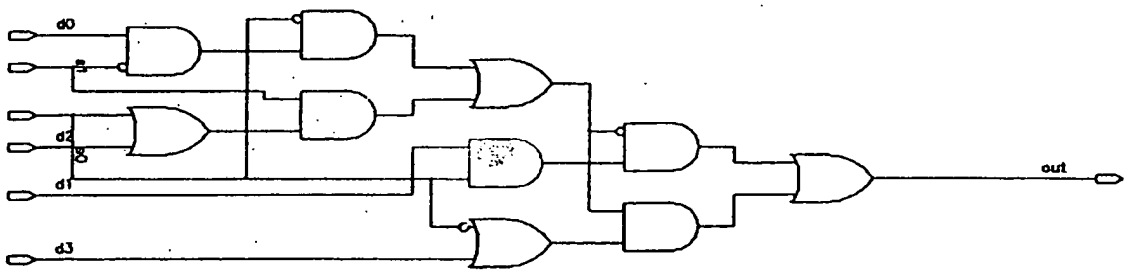

FIGURE 9 *(PRIOR ART)*

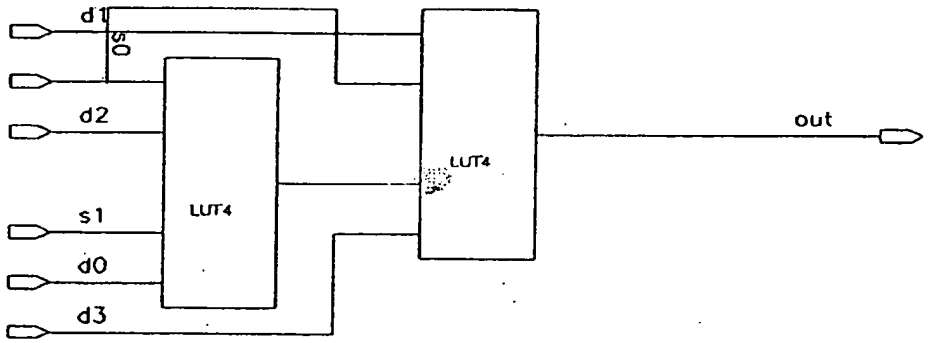

FIGURE 10

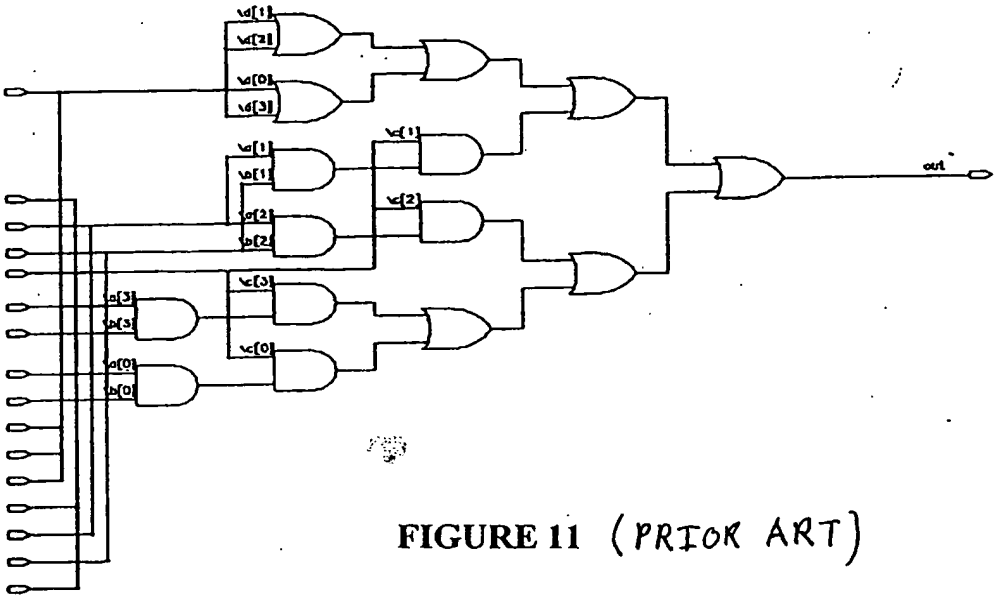

FIGURE 11 (PRIOR ART)

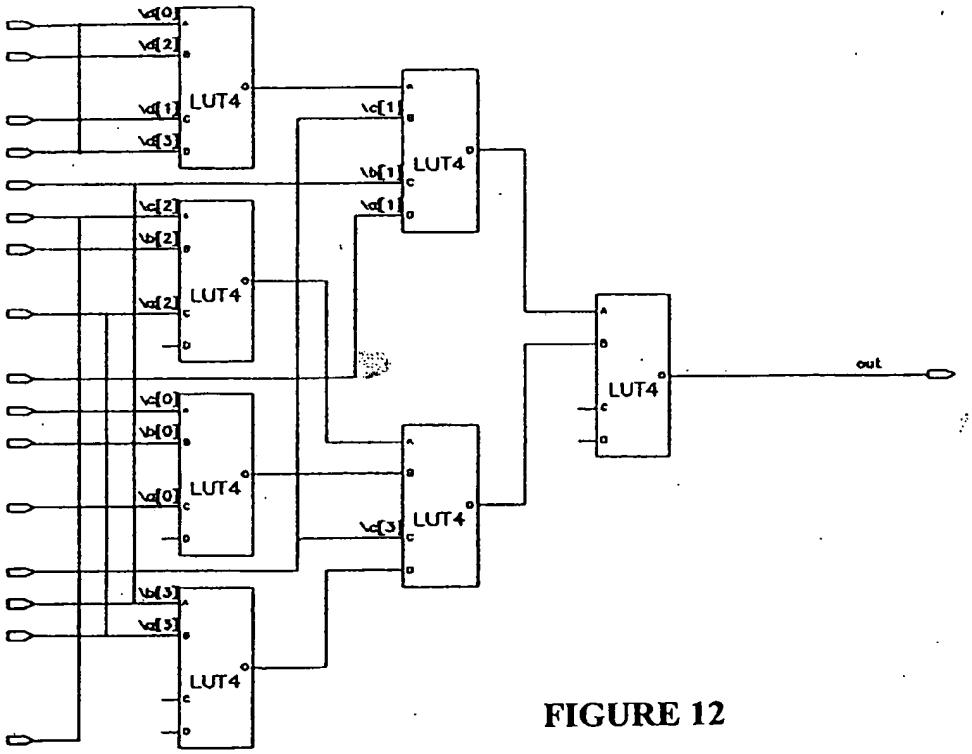

FIGURE 12

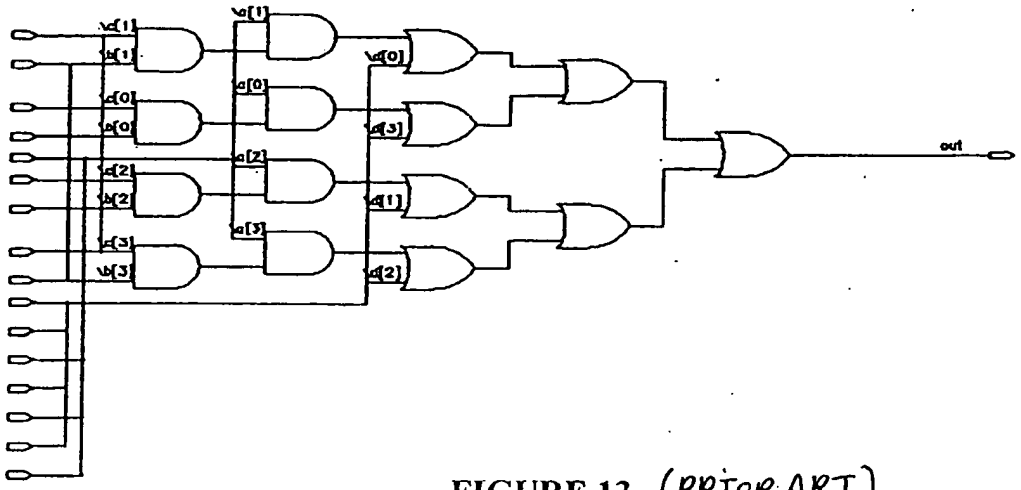

FIGURE 13 (PRIOR ART)

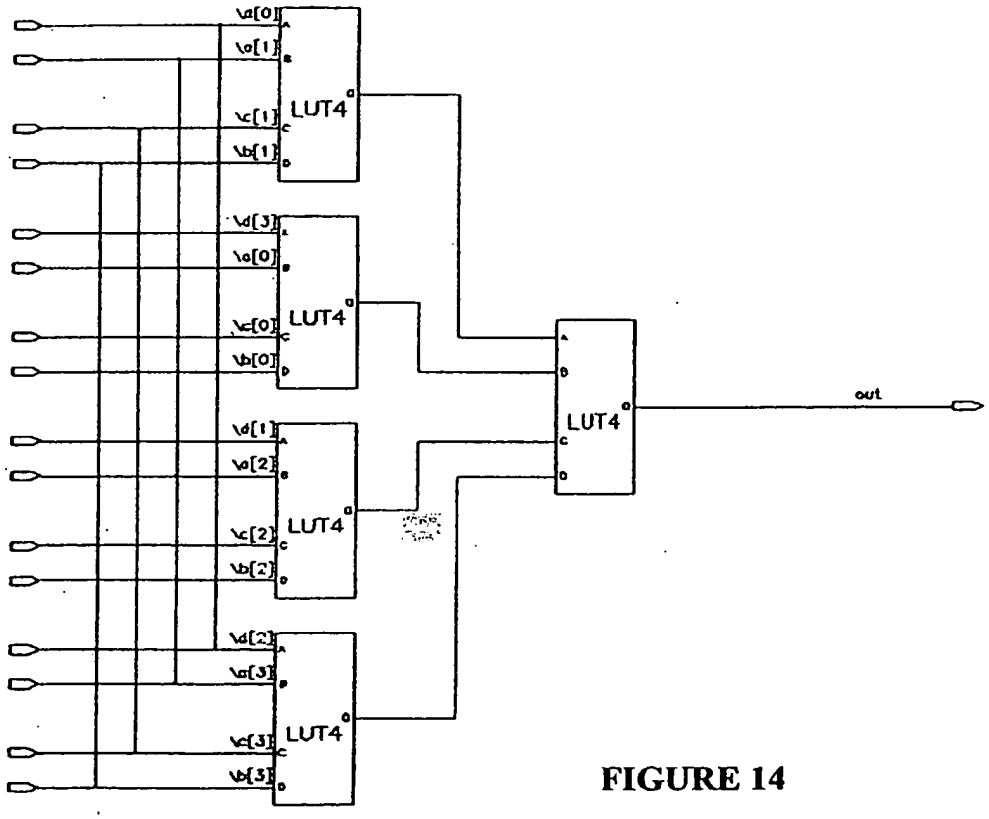

FIGURE 14